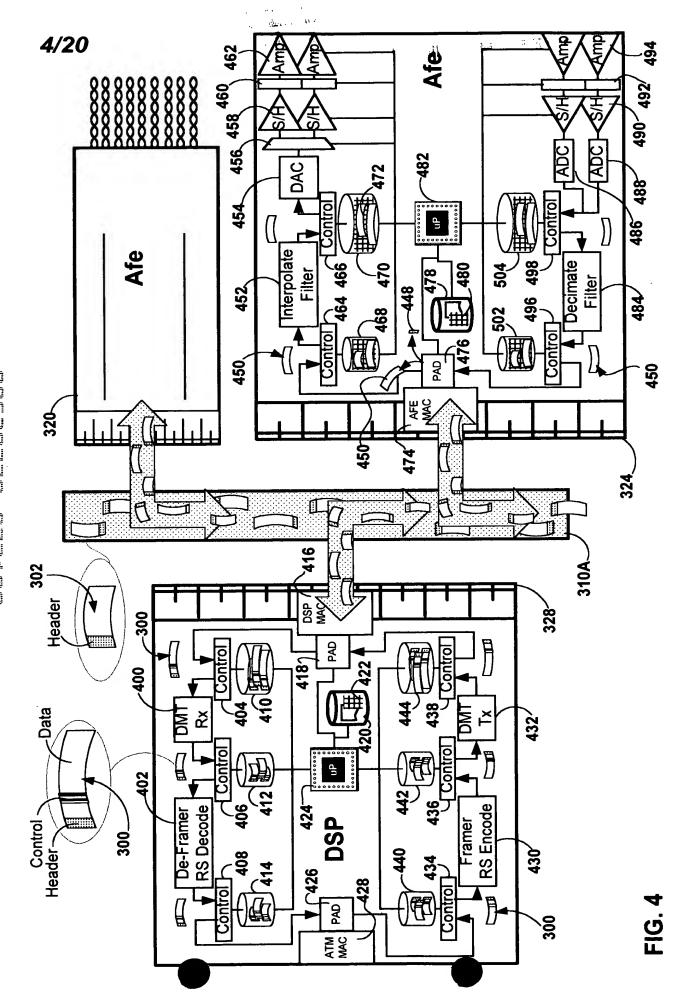
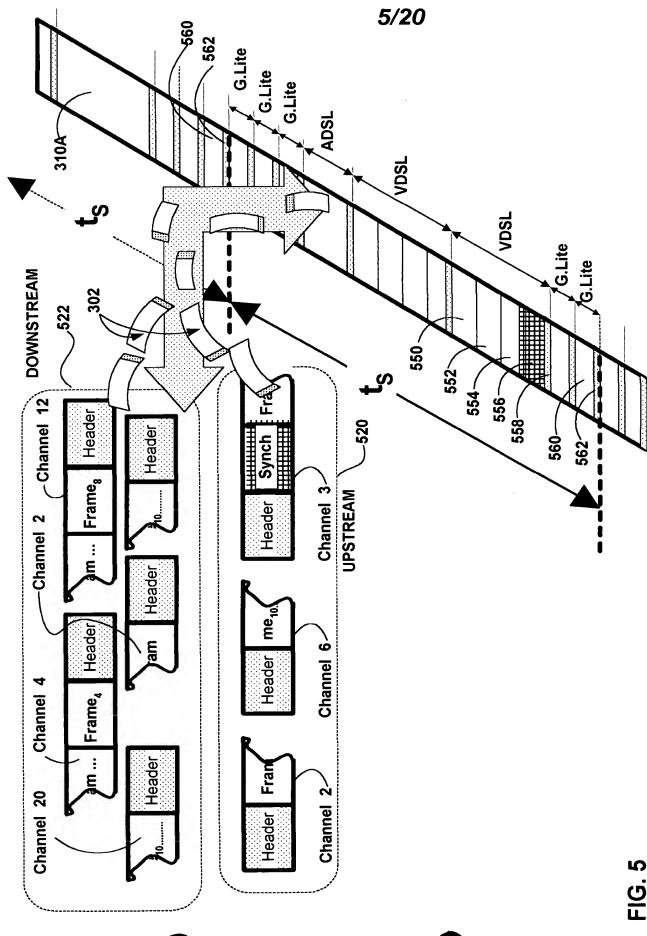


DSECVYS DVELOD

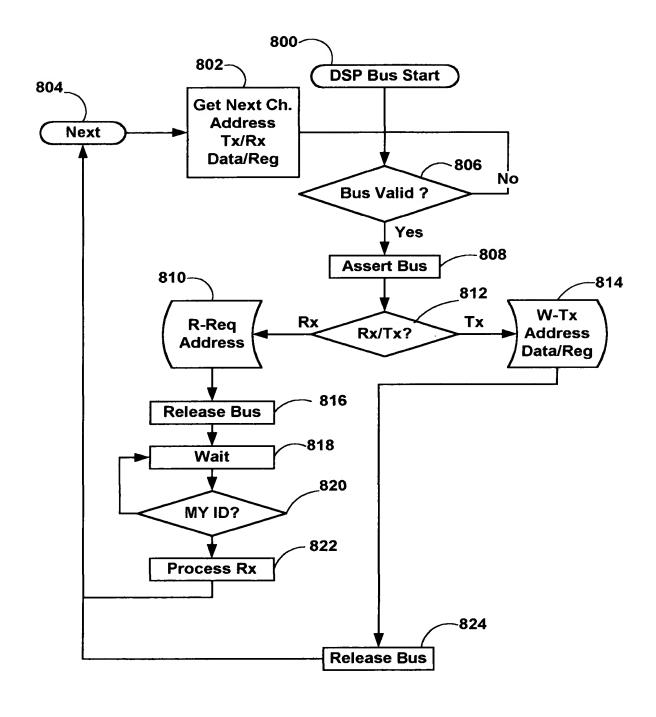


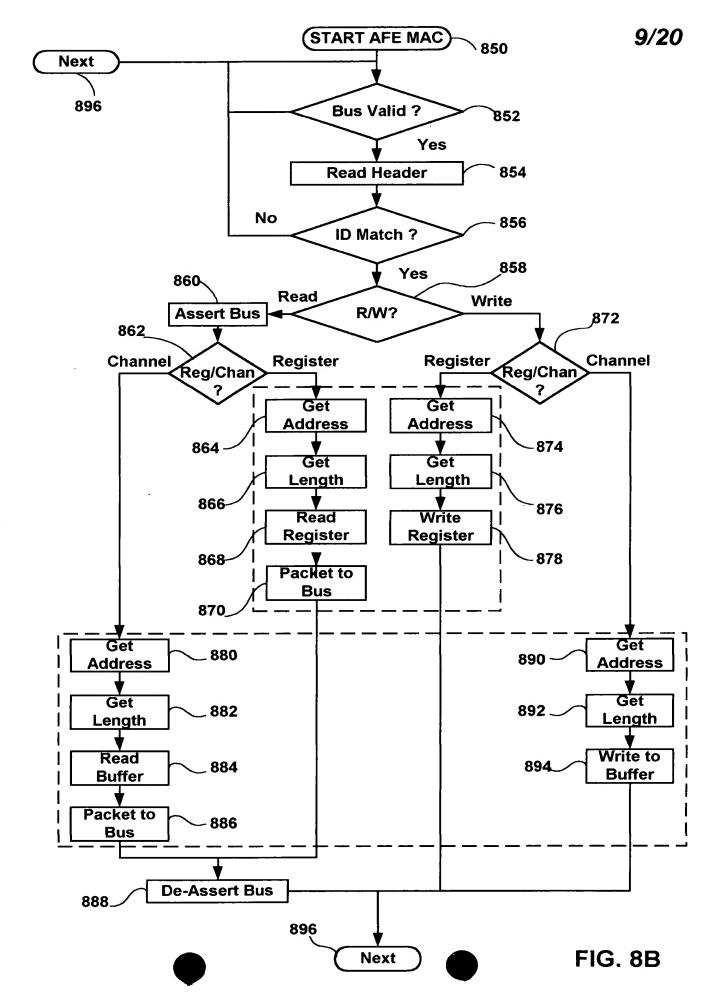


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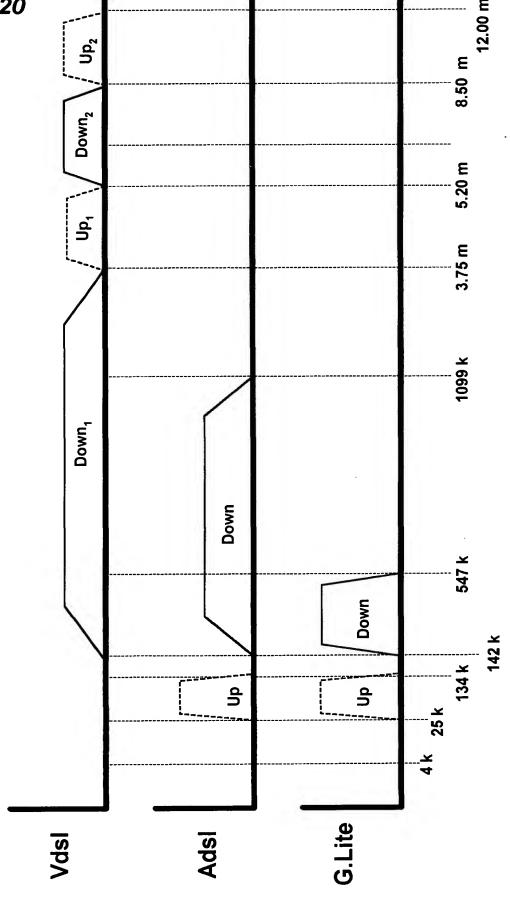
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**~704** Rx Data 724 ZZZZZ KaxHdr 720 TxHdr Tx Data TxHdr 22222 Bus Valid (Pin) Clock Data









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Component Parameters

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Sample space         256         512         1024, 2048, 4096           # Tones         128         256         512, 1024, 2048           Cyclic Prefix         16         32         Programmable           Switching         High Pass         High Pass         High Pass           Filter         Filter         Filter         Filter					
256 512 128 256 16 32 • • • High Pass High Pass Filter Filter		G.LITE	ADSL	NDSL	Other
128 256 16 32 High Pass High Pass Filter Filter	Sample space		512	512, 1024, 2048, 4096	
16 32 High Pass High Pass Filter	# Tones	128	256	256, 512, 1024, 2048	
High Pass High Pass Filter	Cyclic Prefix	16	32	Programmable	
9 High Pass High Pass Filter	••	•	•		
g High Pass High Pass Filter Filter		•	•	•	•
Filter Filter	Switching	High Pass	High Pass		
	0	Filter	Filter	None	

DSP DSP

	_		<del>-</del>							
	4×	3.75 MHz. 8.5MHz		1 Champel	D = 0	11.5 dbm		••		
	& &	1.104 MHz		8 Channels		20.4 dbm		•		
	×	552 kHz		8 Channels 8 Channels		17.4 dbm		•	***	
Information	ii iter polator	Digital Filter	Noise Shaping	DAC	A 222.5	dille	•		Switching	

FIG. 10B

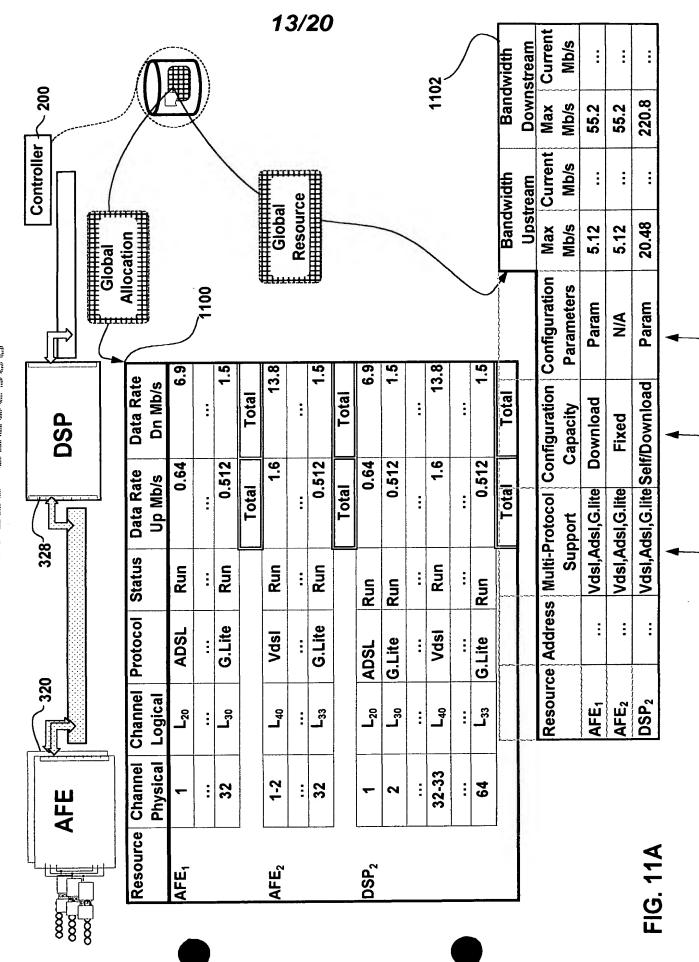
AFE

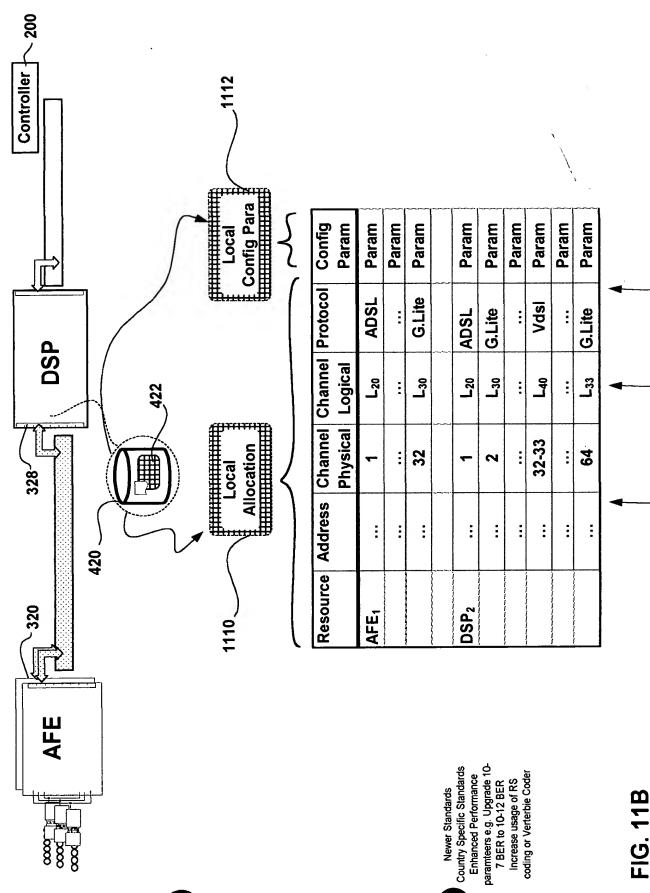
Component Parameters

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FIG. 10C Other 512, 1024, 2048, 4096 256, 512, 1024, 2048 5.2 MHz, 12.0 MHz Programmable 2 x 11 bit Linear VDSL 1 Channel 64x 1bit 64x 1bit SigmaDelta SigmaDelta ADSL 8 Channels | 8 Channels 138 kHz 8 32 4 G.LITE 138 kHz 9 32 4 Sample space Cyclic Prefix Amp Gain Ctrl Switching # Tones Analog Filter Decimator Switching ADC DSP AFE





OSECTES OFEDO

FIG. 11B

